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**COMBINED LUMPED AND CONTINUUM PARAMETER DESIGN OPTIMIZATION OF
ELECTRO-THERMAL SYSTEMS**

**Danny J. Lohan
James T. Allison**

Engineering System Design Laboratory
Department of Systems and Entrepreneurial Engineering
University of Illinois, Urbana, IL 61801
Email: [dlohan2, jtalliso]@illinois.edu

**Ercan M. Dede
Masanori Ishigaki**

Electronics Research Department
Toyota Research Institute of North America
Ann Arbor, MI, 48105
Email: [eric.dede, masanori.ishigaki]@toyota.com

ABSTRACT

In this article we explore a coupled design strategy for the simultaneous optimization of lumped-parameter (electrical) and continuum parameter (thermal) systems. In terms of electrical circuit response, advances in the development of wide band-gap semiconductors and the high speed transient behavior of these devices leads to challenges associated with damping or overshoot. To address such issues, traditional circuit design strategies should evolve to incorporate next generation electrical components effectively. Thus, we propose the incorporated design of circuit layout and routing in conjunction with heat spreader design as a more comprehensive means to optimize the layout of power-dense electronics. The effects of this multidisciplinary design are evaluated by analyzing the Pareto set, which was observed to shift towards the utopia point with each additional design consideration.

1 INTRODUCTION

To address the emergence of wide band-gap semiconductor devices, we propose a coupled design strategy for a lumped parameter electrical circuit model and a continuum thermal model. This is achieved by simultaneously designing a heat spreader with circuit layout to capture the design coupling between the two systems and improve overall performance. In optimizing the performance of the circuit, four distinct design considerations are taken into account: circuit component placement, the routing

of the electrical trace connecting these components, trace shape, and heat spreader topology. These design considerations influence three dependent properties: self-inductance, resistance, and temperature. These properties are then used to evaluate three circuit performance metrics: current overshoot, direct current (DC) loss, and maximum temperature (Fig. 1). Design coupling is due to Joule heating, which is resistive heating that arises from electrical current. Flow of electrical current influences heating and temperature, but temperature influences electrical resistance, which in turn impacts electrical current.

The detrimental effects of heat on circuit performance are well-known and researchers have used co-simulation techniques on a discretized domain to evaluate these effects. Ren et al. used

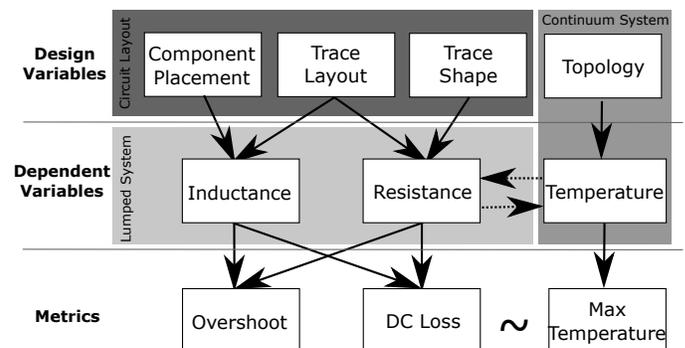


FIGURE 1. Circuit design relationships.

the finite volume method to evaluate the voltage drop and temperature on the domain [1]. Liu et al. used co-simulation to evaluate how heating affects the maximum current that can pass through a wire [2]. Lu and Jin used the Finite Element Tearing and Interconnection method to decrease the computational burden for simulation by decomposing the finite element model and solving spatial domains in parallel [3,4]. As a step towards mitigating thermal effects, Xie and Swaminathan designed the use of through-silicon vias as a tool for improved heat dissipation [5]. Additionally, Dede et al. investigated the use of topology optimization to design electro-thermal circuit trace shielding zones to protect temperature sensitive components [6]. In this work, a co-simulation strategy is used to enforce consistency between a lumped parameter circuit and distributed parameter heated domain. In using this technique, design variables are properly updated to shift towards a system-level optimal solution using both circuit layout and topology optimization.

In optimizing the circuit layout two distinct considerations are taken into account, the first of which is the placement of circuit components. This type of layout optimization problem has been explored by several researchers for different scale problems. Considering a small scale problem, Shook et al. [7] used a lumped thermal system model to predict thermal characteristics on the domain when optimizing the placement of power modules. Hammadi et al. [8] coupled several commercial finite element packages using iSIGHT in the layout optimization of power modules. Transitioning to large-scale problems is difficult, in particular because of the increased number of constraints. Screening methods have been developed to assist engineers in designing a circuit [9, 10], however the task still relies on the engineer to make design decisions. The methods presented here are for small circuit applications, but may be scaled to larger circuits.

The second circuit layout design consideration addressed here is the routing of the conductive trace that connects components. Traditional methods for solving the circuit routing problem rely on a ground structure of nodes and shortest path algorithms to determine the minimum wiring required to connect components together. For large scale circuits, escape routing strategies have been developed to minimize wiring length [11–14]. For smaller circuit problems, inter-component connections are designed using various heuristic-based approaches [15–17]. In the application presented here, inter-component routing is considered with spline representations for the wires. This parameterization of the wire trace allows for design freedom in modifying the geometrically dependent circuit dynamics, resistance, and inductance.

As a final design consideration, a heat spreader will be designed in conjunction with the circuit using topology optimization approaches. Topology optimization strategies have been well-studied across several domains since the seminal paper was published by Bendsoe and Kikuchi [18]. Several researchers have adapted this technique for various applications of heat trans-

fer. When considering steady-state heat conduction for a homogeneously heated domain [19–23], optimal passive heat spreaders resembled branching structures. This tendency is also observed when designing three-dimensional heat spreaders and cold plates [24–26]. In this study, topology optimization techniques are applied to a domain consisting of discrete heat sources where the structure of the optimal heat spreader is unknown.

To assess the effect of each design consideration, multi-objective optimization studies are conducted to develop Pareto sets [27] that are used as targets for the investigation of single level coordination strategies to design these discrete systems [28].

The organization of the paper follows. The next section describes model development and design parameterization for the electrical circuit. A multi-objective study is then presented to develop a benchmark to test the simultaneous electro-thermal design strategy. Topology optimization is then presented and incorporated as a design strategy. The following section presents results when using multi-disciplinary optimization (MDO) strategies to coordinate the design of these coupled but distinct systems. This article then concludes with a discussion of results and future work.

2 Electrical Circuit Analysis

To demonstrate the capability of this design methodology, a case study is selected based on a printed circuit board prototype described in Ref. [29]. Of particular interest is the interface between the main heat generating and electrically sensitive components, the gallium nitride field-effect transistor (GaN FET) switches. The buck converter prototype may be simplified by the graphical procedure illustrated in Fig. 2.

The lumped resistance, R , is a function of the length of each wire trace section and the internal resistance of the switches. It is modeled using the following equation:

$$R = \rho \frac{l}{A_e}, \quad (1)$$

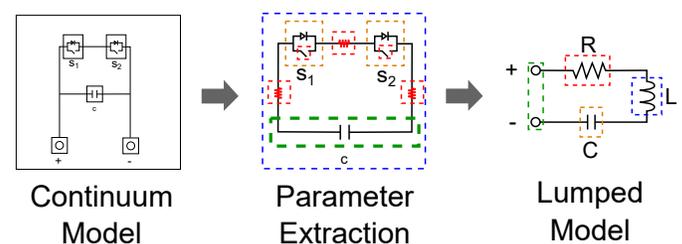


FIGURE 2. Lumped parameter model extraction for RLC equivalent circuit. Note that the dashed orange, blue, green, and red lines represent the equivalent capacitance, inductance, voltage source, and resistance, respectively.

where ρ is the electrical resistivity of the conductor, l is the length of a trace section, and A_e is the effective cross sectional area in which current travels. Both DC current and alternating current (AC) characteristics are observed in the operation of the buck converter. To capture this, two different definitions of A_e will be used based on the mode of operation. While DC current uses the entire wire cross section, AC current migrates to the wire surface. The depth from the surface at which a majority of the AC current flows is called the ‘skin depth’, δ , which is defined as:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \sqrt{\sqrt{1 + (\rho\omega\epsilon)^2} + \rho\omega\epsilon}. \quad (2)$$

The skin depth depends on AC frequency, ω , permittivity of the metal trace, ϵ , and magnetic permeability, μ .

The lumped inductance, L , is computed based on trace layout. Specifically, the self inductance of the wire loop that results when connecting the components together is calculated. The self-inductance of an arbitrarily shaped wire loop may be approximated by the following equation [30]:

$$L = \frac{\mu_0}{4\pi} \left(\oint \frac{d\mathbf{x} \cdot d\mathbf{x}'}{|\mathbf{x} - \mathbf{x}'|} \right)_{|s-s'| > w/2} + \frac{\mu_0}{4\pi} lY + H.O.T., \quad (3)$$

where the self-inductance, L , is given by the boundary integral of one over the norm of each finite segment, s , with respect to every other finite segment, s' . The second term captures the contribution of the skin effect as a function of wire length, l , and skin depth parameter, Y . Given that the inductance must be calculated by a discretized representation of the wire loop, the accuracy of the equation depends on the wire trace width, w . The error of this inductance model tends to zero as w decreases.

The lumped capacitance is derived from the capacitance of the switches, which can be obtained from vendor component data sheets. These simplified models are used to quickly extract the lumped parameters for the circuit and capture the characteristics of a design. Future studies include higher fidelity finite element analysis to increase the accuracy of solutions.

Overshoot and loss metrics for the circuit are calculated based on the following transfer function expressed in the Laplace domain:

$$\frac{V_c(s)}{V(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}, \quad (4)$$

This transfer function compares the output voltage across a switch to the input voltage. Performing analysis in the Laplace

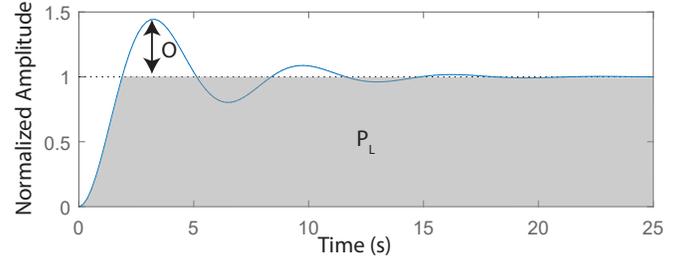


FIGURE 3. Sample second order signal, where overshoot, O , is measured from steady-state value to peak, and DC loss, P_L , is quantified as the sum of the area under the DC signal.

domain supports simple analytical calculation of electrical response metrics. A sample second order response is presented in Fig. 3.

A second order transfer function can be represented using the following general form:

$$G(s) = \frac{\omega_n^2}{s^2 + \zeta\omega_n s + \omega_n^2}, \quad (5)$$

where ω_n is the natural frequency of the system and ζ is the damping coefficient. From the general form, closed form solutions for quantities of interest (Table 1) can be derived as a means to reduce optimization computational cost.

TABLE 1. Metrics for evaluating system performance.

Name	Variable	Expression
Overshoot	O	$e^{-\pi\zeta/\sqrt{1-\zeta^2}}$
DC Loss	P_L	$I_{RMS}^2 R_{DC}$

For a second order system, the overshoot of the system can be found in terms of the damping ratio, ζ . Comparing the structure of the derived transfer function to the general form, ζ is:

$$\zeta = \frac{R_{AC}\sqrt{C}}{2\sqrt{L}}, \quad (6)$$

where R_{AC} is the AC circuit resistance. The DC loss of the system is a function of the root-mean-square current, I_{RMS} , and DC resistance, as loss more closely resembles a steady-state response. These objectives are used in quantifying circuit performance and obtaining a Pareto set. To develop a Pareto front, the following

optimization problem can be solved varying the parameter, α , from 0 to 1.

$$\text{Obj} = \alpha P_L + (1 - \alpha)O \quad (7)$$

When optimizing the system, varying α produces various types of structures. This weighted-sum strategy for multi-objective optimization does have some disadvantages, including inability to resolve non-convex portions of Pareto fronts. The multi-objective optimization studies presented in this article were performed instead using the MATLAB[®] multi-objective genetic algorithm (MOGA) tool, `gamultiobj`. In addition to providing an effective means for identifying points in the Pareto set, `gamultiobj` also improves the probability of finding globally-optimal solutions.

2.1 Co-simulation Strategy

To evaluate the performance of the system properly with respect to heating considerations, a co-simulation strategy was used. Both the lumped and distributed parameter models are solved iteratively (fixed-point iteration [28]) to achieve agreement in thermal response. The power loss of each switch and section of trace wire is distributed equally to each representative element in the continuum model. This is used as a load input for the finite element analysis used to solve for the temperature response on the domain. The mean temperature of the elements for each switch and trace wire is returned to the lumped circuit model for re-evaluation. The convergence criterion for this iterative analysis is:

$$\text{mean}(T(i) - T(i-1))^2 \leq \xi \quad (8)$$

where: $T(i) = [T_{s1}(i), T_{s2}(i), T_{r1}(i), T_{r2}(i), T_{r3}(i)]$.

The co-simulation technique is repeated between the lumped parameter and continuum model until the square of the mean change in temperatures is less than a specified tolerance, ξ . In Eqn. (8), $T(i)$ is a vector consisting of the mean temperature of each switch and section of trace wire at iteration, i . This guarantees that the temperature of each discrete object converges within the tolerance, ξ . The co-simulation analysis is shared between all optimization routines to ensure accurate evaluation.

2.2 Circuit Layout Design

The circuit layout here is defined by the location of each component and the routing of the trace connecting the components. When these geometric properties are modified, the lumped parameters of the circuit are updated. In this design problem, system architecture is fixed (the set of components and connections

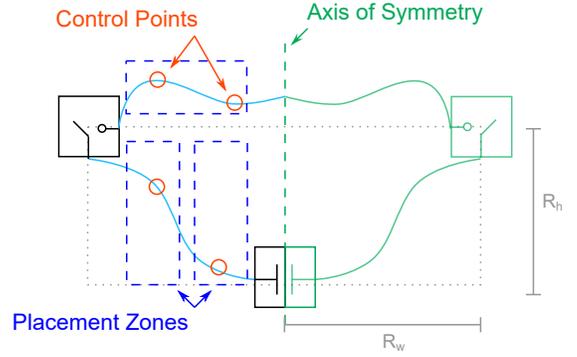


FIGURE 4. Circuit layout parameterization using optimized device position and trace spline control point design variables.

does not change). The two switches are placed at the upper vertices of a rectangle and the capacitor is placed in the center of the lower length as shown in Fig. 4.

Early experimentation revealed the symmetric tendencies of optimal designs. Enforcing symmetry via design representation reduces the component placement design description dimension to two design variables, as illustrated by R_v and R_w in Fig. 4. The trace wires that connect each pair of components are parameterized by vertices, referred to as control points. A spline that represents trace wire routing path is fit from one component through its control points to the paired component. The control points are restricted to separate zones to ensure the trace remains within a boundary which prevents overlap. The number of control points that represent a spline can be changed to vary available spline geometry complexity and allow access to other sections of the design domain. The design vector, \mathbf{x}_E , for the electrical system is:

$$\mathbf{x}_E = [R_w, R_h, c_{1x}, c_{1y}, c_{2x}, c_{2y}, \dots, c_{nx}, c_{ny}], \quad (9)$$

where component locations are specified by R_w and R_h , and the trace geometry is specified by the x and y coordinates of the n control points c .

Based on these design considerations, a multi-objective optimization study can be performed to develop an initial Pareto set. The results of this study when using different spline resolutions are presented in Fig. 5.

The ideal design performance for a multi-objective design optimization study is the utopia point, a (normally unattainable) design that achieves the best possible values for all objective functions simultaneously based on the best values obtained if each objective function was optimized individually (i.e., the anchor points). In realistic multi-objective problems the utopia point is unattainable because the objectives conflict. Pareto fronts quantify the tradeoffs between conflicting objective func-

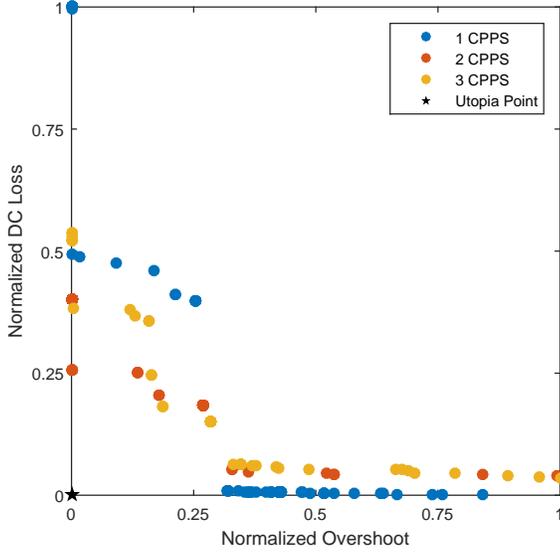


FIGURE 5. Pareto front of optimal circuit designs for three distinct spline resolutions.

tions. Shifting to better design strategies or technologies often can shift the entire Pareto front closer to the utopia point (a desirable result).

The multi-objective optimization study was repeated for three different spline resolutions, with 1-3 control points per spline (CPPS). Increasing the available complexity of the spline makes possible the shifting of the Pareto front closer to the utopia point. For this particular problem, Pareto front shifts are possible because lower CPPS values cannot access higher-performing design geometries. The 2 CCPS spline representation provides reasonable design space coverage, so it was chosen as the basis for subsequent studies. When analyzing Fig. 5, it can be seen that the chosen objectives, overshoot and DC loss, are competing objectives. Increasing one objective function will degrade the other. Improving both simultaneously (i.e., a Pareto front shift) can be realized by exploring design changes beyond component location and trace routing.

2.3 Trace Shape Design

In addition to component placement and trace routing, changes to trace shape design were considered as well. When traveling through a wire, a majority of the electrons in alternating current travel at the surface of the wire. This results in a difference between AC and DC resistance values. Since AC resistance has significant dynamic effects on damping, designing the trace shape to optimize these effects is desirable. Consider the parameterization presented in Fig. 6 where the trace can have rectangular protuberances extending from the trace path.

Given a bounded design domain, or path of trace wire, the

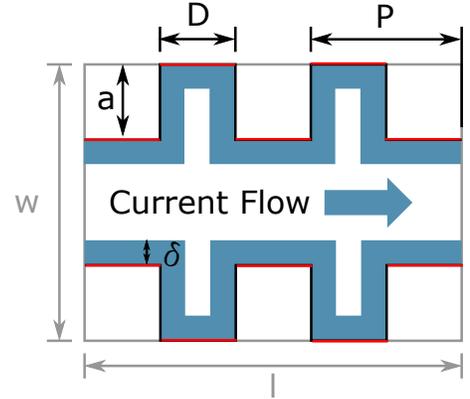


FIGURE 6. Circuit trace parameterization where DC current flows through the middle rectangle and AC current flows along the blue path.

gap between AC and DC resistance can be modeled in a simplified way by comparing perimeter and area. DC current travels through the smallest uniform cross section of the wire which is thus used to calculate DC resistance:

$$R_{DC} = \rho \frac{l}{w - 2a}. \quad (10)$$

The effective area of the cross section is the difference between the wire width w and total lateral size of the square features, $2a$. Since AC current only travels through the surface of the wire, designs that increase the path length of AC current travel will increase AC resistance. This can be approximated by the following equation:

$$R_{AC} = \rho \frac{l + 2na}{2\delta}, \quad (11)$$

where the number of square features, n , is chosen to be large enough to maintain the surface current effect of AC current. If the number of square features along the spline is held fixed at the maximum allowable number, this creates a one dimensional problem that can be solved in terms of feature height, a , to achieve a desired damping increase. The rate of increase of AC and DC resistance while varying a is visualized in Fig. 7.

This chart may be used to select the maximum amount of AC resistance that can be achieved for a given increase in DC resistance. For small changes in DC resistance, large changes in AC resistance can be obtained. As a demonstration of the concept, a minimum DC loss design was obtained and is shown in Fig. 8. The trace paths connect components with minimum path length for the two control point parameterization, and square features are added to the trace wire to tune AC resistance.

We would like to use trace shape design as a mechanism to help shift the Pareto front. Specifically, maximizing the gap

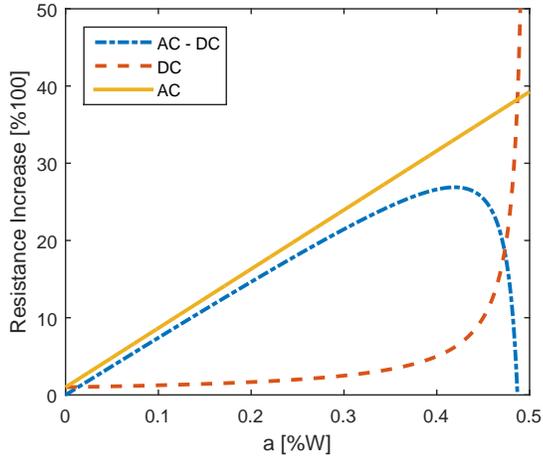


FIGURE 7. Trace design resistance comparison.

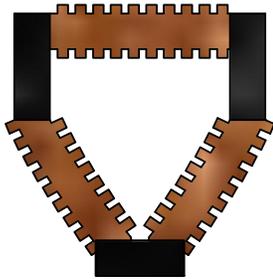


FIGURE 8. Circuit trace shape design with square features to increase AC resistance.

between AC and DC resistance should help accomplish this by allowing for the best possible damping effect. Repeating this study with the extended design flexibility of trace shape design did in fact result in a Pareto front shift as shown in Fig. 9.

When including trace shape design, optimal designs are observed that perform worse in DC loss. However, designs that perform better in overshoot are also observed. This is due to the increase in AC and DC resistance accessible through wire trace shape adjustments. To address the increase in DC loss, heat spreader design will now be considered in addition to the circuit layout and trace shape optimization.

3 Heat Spreader Design

To augment the circuit design problem that addresses electrical system performance, the design of a heat spreader will be considered to help improve thermal performance. The circuit design problem is formulated using a lumped parameter model, and the heat spreader design problem is formulated using a distributed parameter (continuum system) model. It will be shown

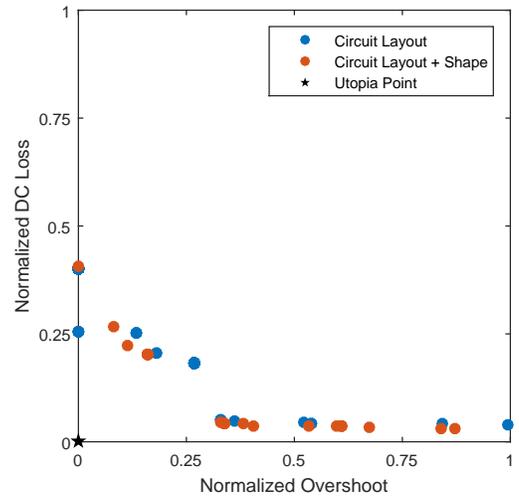


FIGURE 9. Pareto fronts of optimal circuit designs with and without trace shape design. Adding trace shape design results in overall performance improvement.

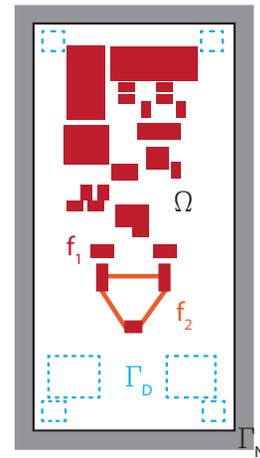


FIGURE 10. Circuit continuum representation for heat spreader design.

that incorporating electrical and thermal systems together into a single simultaneous design optimization problem further improves system performance. The heat spreader will be placed within a multi-layer printed circuit board. To understand heat spreader design, consider the diagram in Fig. 10 that depicts the heat conduction aspects of a sample circuit.

The power loss of the circuit is realized as component and Joule heat, f_1 and f_2 , respectively (Eqn. (12) below). This heat is transferred to the heat spreader, which is modeled as a continuum

system. Here we assume that the entire domain boundary Γ_N is adiabatic. In the present problem there are several sinks present on the design domain Γ_D . The general goal of heat spreader design is to extract as much heat as possible from the domain to ensure the integrity of the electronic components. As a means of designing the heat spreader efficiently (i.e., maximum thermal performance for a given amount of material), a topology optimization strategy is implemented.

$$\nabla \cdot (k(\gamma)\nabla T) + f_1 + f_2 = 0 \text{ on } \Omega, \quad (12)$$

$$T = 0 \text{ on } \Gamma_D, \quad (13)$$

$$(k\nabla T) \cdot \mathbf{n} = 0 \text{ on } \Gamma_N, \quad (14)$$

3.1 Topology Optimization

Continuum topology optimization determines the optimal allocation of material on a design domain. This is done by discretizing the design domain into finite elements and assigning a material density, $0 \leq \gamma_i \leq 1$, to each finite element. A common type of objective function used in topology optimization problems is a compliance metric. Thermal compliance is associated with the degree of heat extraction, and the widespread use of this objective is due to its simple and inexpensive gradient calculation. An exploration of heat spreader design problem formulations for printed circuit board applications was recently conducted by the authors [31]. For the purpose of the studies here, the maximum temperature was chosen as an objective. This aligns well with the power loss objective and promotes a circuit board with desirable low temperatures. Direct consideration of electrical performance in topology optimization is a topic for future work, possibly utilizing generative design strategies that support more general formulations [23].

The topology optimization problem considered here is:

$$\min_{\mathbf{x}_T} \max(T) \quad (15)$$

$$\text{s. t. } V(\mathbf{x}_T) = V_p \quad (16)$$

$$R(\mathbf{x}_T) \geq R_{\min}, \quad (17)$$

where $\mathbf{x}_T = [\gamma_1, \gamma_2, \dots, \gamma_{n_E}]^T$ is the thermal system design vector and n_E is the number of elements in the design domain.

A fixed volume constraint, $V(\mathbf{x}_T) = V_p$, must be satisfied, and a manufacturing constraint ensuring a minimum member radius, R_{\min} , is observed. To solve this problem the Solid Isotropic Microstructure with Penalization (SIMP) method is used. The SIMP method uses continuous density variables for each cell. This enables use of efficient gradient-based optimization methods, but presents the challenge of cells with intermediate density. SIMP addresses this by penalizing elements away from intermediate density values, resulting in cells that are approximately void ($\gamma_i \approx 0$) or full density ($\gamma_i \approx 1$) [19]. In this problem 0 represents an element with non-conductive material (FR-4) and 1 represents

an element with conductive material (copper). When optimizing the heat spreader design for a given circuit with various volume constraints, different structures can be observed as shown in Fig. 11.

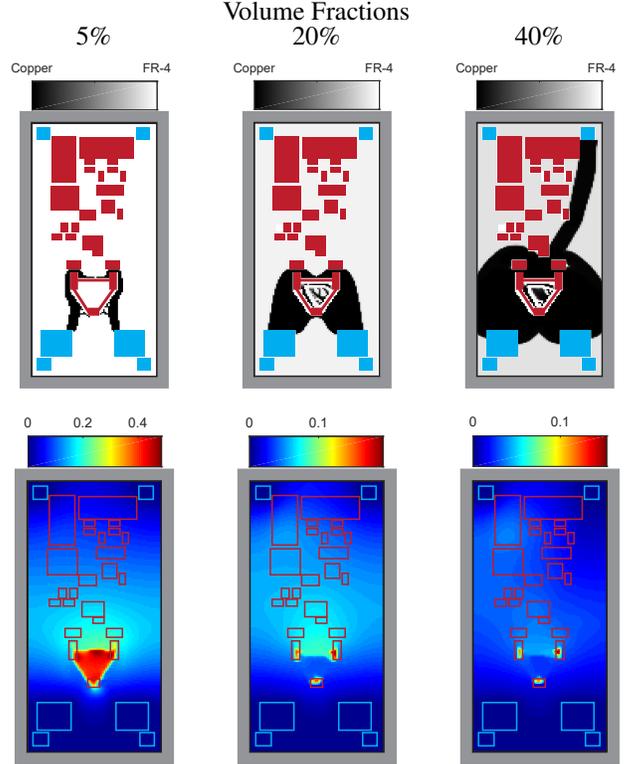


FIGURE 11. Heat spreader designs (top). Dark regions indicate solid conductive material and light regions indicate void. Normalized temperature maps (bottom). Red regions are hot and blue regions are cool.

By varying V_p we can identify the minimum conductive material volume fraction that provides acceptable heat extraction. Figure 12 shows how maximum domain temperature varies with volume fraction for a fixed circuit design. Though this may not hold for all circuit layout designs, it is clear that beyond $V_p = 20\%$, further increase in volume fraction does not reduce maximum domain temperature significantly for this design.

To use SIMP with the multi-objective genetic algorithm available in MATLAB[®], a nested formulation is used. For each candidate circuit design tested by the outer loop, the optimal heat spreader design is found using SIMP. The resulting Pareto front is compared to previous results in Fig. 13

Once again, adding a new design consideration (heat spreader design here) shifts the Pareto set closer to the utopia point. The use of a heat spreader reduces circuit losses since temperature influences DC resistance. Though DC loss appears

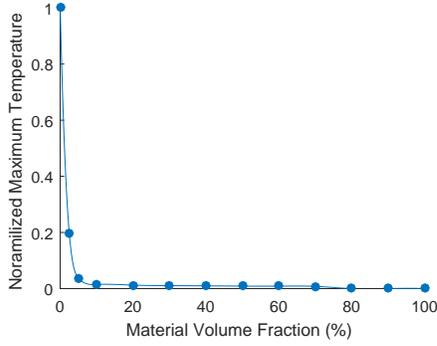


FIGURE 12. Maximum temperature vs volume fraction.

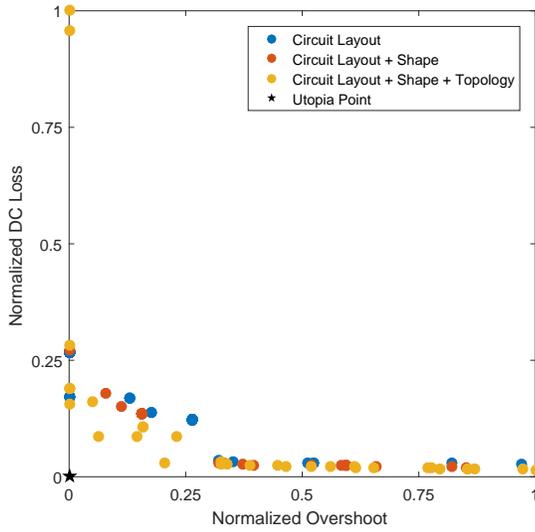


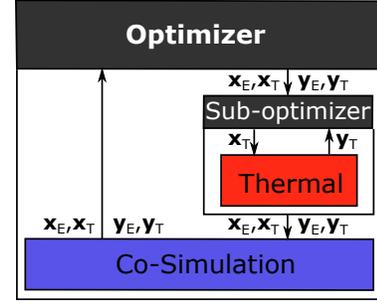
FIGURE 13. Pareto front of optimal circuit designs when using 3 sets of design considerations.

to improve, overshoot remains largely the same.

4 Pareto Set Refinement

While genetic algorithms (GAs) improve efforts to identify global optima, and can generate Pareto sets through a single algorithm execution, GA solutions cannot be proven to be optimal. In addition, solution precision is often low. Identifying one or more anchor points using gradient-based algorithms may help improve confidence in MOGA results if these points are consistent with the MOGA-generated Pareto fronts. In this section we present results from using gradient based optimization techniques to identify minimal DC loss designs (lower right anchor point in the Pareto sets here). Two different coordination strategies were used: nested and simultaneous.

The nested design strategy was described above, but used



(a) Nested formulation



(b) Simultaneous formulation

FIGURE 14. Candidate solution methods for the combined circuit and heat spreader design problem.

MOGA for the outer-loop solution. Here a gradient-based method is used for both inner and outer loops. For each candidate electrical system design, the optimal heat spreader will be found and used in evaluation. The information flow of this procedure is illustrated in Fig. 14(a). Though this strategy guarantees a feasible design at each iteration, it requires many function evaluations for convergence. In implementing this strategy, the MATLAB[®] function `fmincon` is used to update the circuit design parameters, and the method of moving asymptotes (MMA) is used as the SIMP solver to converge quickly on a heat spreader design for each candidate circuit layout.

The simultaneous strategy solves a single optimization problem for both sets of design variables concurrently. When using simultaneous optimization, feasibility with respect to design constraints is not guaranteed until optimization convergence. Both the circuit and heat spreader design variables are optimized using the MATLAB[®] function `fmincon`. The gradients for the circuit design problem are calculated using forward finite differencing as defined by the following formula:

$$\Delta P_L = \frac{P_L(x+h) - P_L(x)}{h}, \quad (18)$$

where the change in the loss for a circuit layout is measured once for each small perturbation h . Gradients for the heat spreader are calculated using analytical sensitivity analysis [32]. To improve the convergence characteristics of this problem, the gradients of the circuit layout are scaled adaptively to match the order of the topology optimization problem. The simultaneous strategy requires that multidisciplinary analysis is performed via

co-simulation.

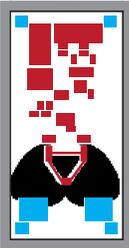
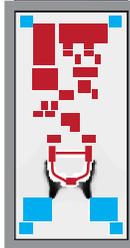
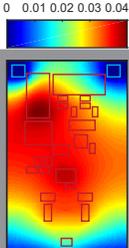
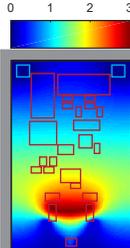
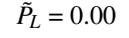
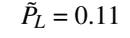
To test the effectiveness of each strategy, numerical experiments were conducted to achieve the minimum loss designs. A multi-start approach was used to improve the probability of finding a globally-optimal design. The results from each strategy are presented in Table 2.

When using the nested coordination strategy, the algorithm performs well when optimizing for minimum loss. The performance value obtained is the best result and lies just below the Pareto curve obtained using MOGA. The simultaneous design strategy, however, was not able to produce the same result. The optimal circuit layout and heat spreader topology have difficulty converging to the optimal designs. This is evident from the amount of intermediate density material (gray-scale) throughout most of the domain for the simultaneous result shown in Table 2.

5 Conclusion

This initial study has revealed many insights pertaining to coupled electro-thermal system design. In using a lumped and continuum model co-simulation strategy, the effects of design coupling are apparent as the design choices in one domain clearly

TABLE 2. Comparison of optimization results using nested and simultaneous coordination strategies for DC loss minimization. Note the differing temperature scales.

	Copper	FR-4	Copper	FR-4
Topology				
Temperature				
Value	$\tilde{P}_L = 0.00$		$\tilde{P}_L = 0.11$	
Coordination	Nested		Simultaneous	

affected the results in the other. This is observed in the multi-objective optimization studies where the Pareto front shifts towards the utopia point when incorporating additional design elements into the optimization problem. This highlights the importance of including thermal considerations when designing for electrical efficiency. Though initial results are promising, there are several issues to address that may help improve simulation accuracy and design performance.

When using the simultaneous coordination strategy with gradient-based optimization, it was difficult to obtain solutions as good as those obtained via MOGA. A possible strategy to address this is to reformulate the topology optimization routine to inherently consider the electrical efficiency of the lumped system. In this way, gradient-based updates may converge more smoothly. In addition to this convergence issue, there is inaccuracy in the line integral equation used to approximate the inductance of a wire loop with large radius. Future work will investigate a continuum finite element strategy for approximating loop self-inductance.

Exploring complex heat spreader designs is also of interest. It was shown that when using heat spreader design minimizing the maximum temperature on the domain, the temperature of the trace wire was reduced considerably. This may create adverse effects by reducing the damping of the dynamic electrical response. In designing the trace layout and shape for damping, this distributed heat source is easy to cool. Designing a heat spreader which targets sensitive components, but avoids the distributed wire heat, may exhibit in a more robust system which has both good damping characteristics and retains a low temperature for heat sensitive components. This type of design exploration would be possible if topology optimization was driven directly by electrical system performance instead of pseudo objectives.

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